

U.S. Patent Application Serial No. 10/612,990  
Response filed May 27, 2007  
Reply to OA dated November 28, 2006

### **REMARKS**

Claims 2 - 10 are canceled without prejudice or disclaimer.

Claim 1 has been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicant regards as his invention. The applicant respectfully submits that no new matter has been added. It is believed that this Response is fully responsive to the Office Action dated November 28, 2006.

The applicant thanks the Examiner for having removed Hiraoka as a reference. The Examiner has now rejected claim 1 in view of a newly cited reference. Details of the rejection are discussed below.

Claim 1 is rejected under 35 USC § 112, first paragraph, as failing to comply with the written description requirement. The Examiner alleges that the claimed insulating layers being of a non-porous material is not disclosed in the originally filed disclosure. The applicant respectfully requests reconsideration of this rejection.

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In view of the Examiner's position on the claimed insulating layers, the applicant has removed such description, objected to by the Examiner, from claim 1. Accordingly, the withdrawal of the outstanding rejection under 35 USC § 112, first paragraph, is in order, and is therefore respectfully solicited.

As to the merits of this case, claim 1 is rejected under 35 USC §102 (e) as being anticipated by U.S. Patent No. 6,274,821 (Echigo). The applicant respectfully requests reconsideration of this rejection.

The applicant's claimed invention, as now recited in independent claim 1, is directed to a multilayer circuit board, which includes a plurality of cable layers, each of which includes electric conductive sections; and a plurality of first insulating layers, each of which encloses the electric conductive sections in each cable layer and fills spaces between the electric conductive sections, each of the electric conductive sections of each of the cable layers including a cable pattern and a land pad. The claimed multilayer circuit board, as now recited in independent claim 1, further includes post vias electrically connecting the electric conductive sections in one cable layer to those in another cable layer, wherein height of the electric conductive sections in each cable layer are equal to that of the first insulating layer enclosing the electric conductive sections. The claimed multilayer circuit board, as now recited in independent claim 1, also includes a second insulating layer, which is formed to enclose the post vias, wherein height of the post vias are equal to that of the second

insulating layer, and each first insulating layer and each second insulating layer are made up of a film covered with an insulating material.

Significant structural arrangements of the applicant's claimed multilayer circuit board, as now recited in independent claim 1, include the claimed a second insulating layer, which is formed to enclose the post vias, wherein height of the post vias are equal to that of the second insulating layer, and each first insulating layer and each second insulating layer are made up of a film covered with an insulating material.

The Examiner alleges that Echigo discloses the claimed invention and refers to Figure 1 as showing the claimed multilayer circuit board.

Echigo discloses many resin materials for use in forming layers of a multilayer printed circuit board. The resin materials are selected to have physical properties that provide a shock-resistive printed circuit.

Echigo does not however describe a method for forming the layers and does not disclose in the text that the heights of electric conductive sections are equal to the height of a first insulating layer enclosing them, and that the heights of post vias are equal to the height of a second insulating layer enclosing them. The Examiner is relying solely on Figure 1 for showing such height

relationships.

In view of the Examiner's position, claim language is needed to distinguish over Echigo, as well as Hiraoka, as the amendment to claim 1, which appears to be necessary to overcome the present rejection under 35 USC §112, first paragraph, would eliminate the language added to claim 1 in the previous response, which provided a distinction between the claimed invention and the device of Hiraoka.

It is noted in the present specification that the claimed insulating layers are formed, for example, by laminating an insulating film made up of polyethylene film covered with an insulating material (page 11, lines 15 - 23). Defining the insulating layers of claim 1 to be comprised of a film covered with an insulating material distinguish the instant claimed invention over the cited prior art mentioned above.

Accordingly, not all of the claimed elements or features, now recited in claim 1, are found in exactly the same situation and united in the same way to perform the identical function in Echigo's device. Thus, there can be no anticipation of the claimed invention based on the teachings of Echigo.

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In view of the above, the withdrawal of the outstanding anticipation rejection under 35 USC §102 (e) based on U.S. Patent No. 6,274,821 (Echigo) is in order, and is therefore respectfully solicited.

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

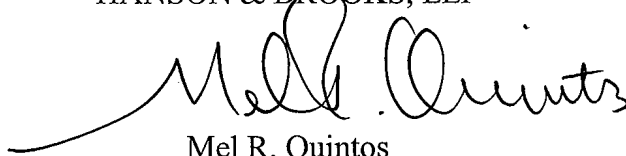
If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

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In the event that this paper is not timely filed, the applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper to Deposit Account No. 01-2340.

Respectfully submitted,

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